TP44100SG-TPPFC+LLC300-EVB

300W Totem-Pole PFC and LLC Resonant Converter using
Tagore Technology's Superior GaN FETs (TP44100SG and TP44200SG)

Rev-1.0

2022-December-16

powergan@tagoretech.com

About this document

Objective and Purpose

This application note describes Tagore Technology's 300W Totem-Pole PFC (TPPFC) + LLC Resonant Converter Evaluation Board (TP44100SG-TPPFC+LLC300-EVB) using its superior GaN FETs TP44100SG (90 mΩ) for the TPPFC section, and TP44200SG (180 mΩ) for the LLC section. The user will be able to perform a complete evaluation of the EVB by following the procedures outlined in this document and all the necessary supporting information (circuit schematics, BOM, layout, key operating waveforms, etc.) is provided to facilitate a quick adaption to a production design.

Intended audience

This application note is intended for Tagore Technology's customers and partners using its 90 *m*Ω and 180 *m*Ω superior GaN FETs TP44100SG and TP44200SG in various power converter applications such as PFC, LLC, half-bridge and full-bridge DC-DC converter applications.

TABLE OF CONTENTS

1 Introduction 5

2 EVB details and its operation 5

2.1 Board images and dimensions 5

2.2 Component markups 6

2.3 Topology and functional block diagram 6

2.4 Specifications 7

3 Connections and Start-Up Procedure 7

3.1 Operating procedure 8

4 Experimental results 8

4.1 Load transient waveforms 9

4.2 Output voltage ripple (ΔV_o) 9

5 Performance data 10

5.1 Efficiency data 10

5.2 Load regulation 11

5.3 Thermal data 11

6 PCB schematic 12

7 PCB Layout and assembly 12

8 Bill of Materials 12

9 Revision history 13

List of Figures

Figure 1: 300W TPPFC and LLC Evaluation board…….5

Figure 2: TPPFC power board (Top left and right) and LLC power board (Bottom left and right)…….6

Figure 3: Block diagram representation of the 300W EVB……..7

Figure 4: 300W Evaluation board test setup…….8

Figure 5: 300W EVB load dynamic response (0 to 100% load and vice-versa)……. 9

Figure 6: Output voltage Vo at no-load (left) and its corresponding ripple voltage ΔVo (right)……...9

Figure 7: Output voltage Vo at full load (left) and its corresponding ripple voltage ΔVo (right)……..10

Figure 8: Efficiency vs output power at 115 Vac and 230 Vac inputs, and 20 V DC output……10

Figure 9: Output voltage vs load current……11

Figure 10: TPPFC and LLC GaN FET's case temperature rise over time under worst case scenarios…….11

Figure 11: Thermal images of the bottom sides of TPPFC and LLC boards after 45 mins of operation……..12

1 INTRODUCTION

A galvanically-isolated AC-DC power converter is widely used in most power supply applications including battery charger, mobile and laptop adaptors, and server power supplies. The converter takes the power from the AC input mains (grid), processes it internally, and feeds it to the load with DC voltage as per the specification. The power train mainly consists of a non-isolated AC-DC front-end converter, which is followed by an isolated DC-DC converter. The latter uses a High-Frequency (HF) transformer, which provides the necessary galvanic isolation between the input (AC side) and the final DC output.

There are many topology options for both the AC-DC and DC-DC converter stages. In this reference design, we have used a Totem-Pole PFC (TPPFC) topology for the front-end AC-DC converter, and an LLC resonant converter topology for the second-stage DC-DC converter. The TPPFC takes the power from the grid and internally generates a stable 400V DC bus, which the LLC stage uses as its input. The LLC resonant converter processes it and outputs a 20V regulated DC voltage across its output terminals.

The use of Tagore Technology's Superior GaN FETs, TP44100SG and TP44200SG, have helped achieve higher power conversion efficiency in comparison to power converters using Si MOSFETs.

2 EVB DETAILS AND ITS OPERATION

The 300W EVB consists of a TPPFC PCB and an LLC PCB, stacked one over another as shown in Fig. 1. The details of the TPPFC PCB are given in the application specific evaluation board – *TP44100SG-TPPFC240-EVB*. For the LLC PCB, please refer to the application specific evaluation board – *TP44400SG-LLC240-EVB1*. The only interconnection between the PCBs is the DC link connections, taken through header pins, as shown in Fig. 1.

2.1 BOARD IMAGES AND DIMENSIONS

A 3D image of the 300W EVB is shown in Fig. 1, where the TPPFC PCB is on the top and LLC PCB is at the bottom. It has a dimension of 10.2 cm × 8.3 cm × 4.3 cm (L x W x H), and a volume of 364 cc.

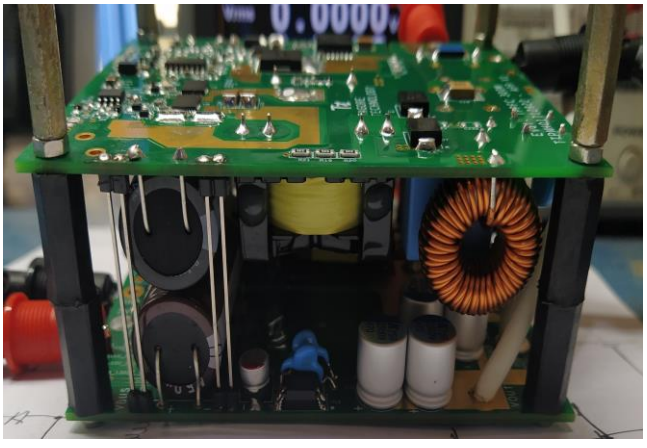

Figure 1: 300W TPPFC and LLC Evaluation board.

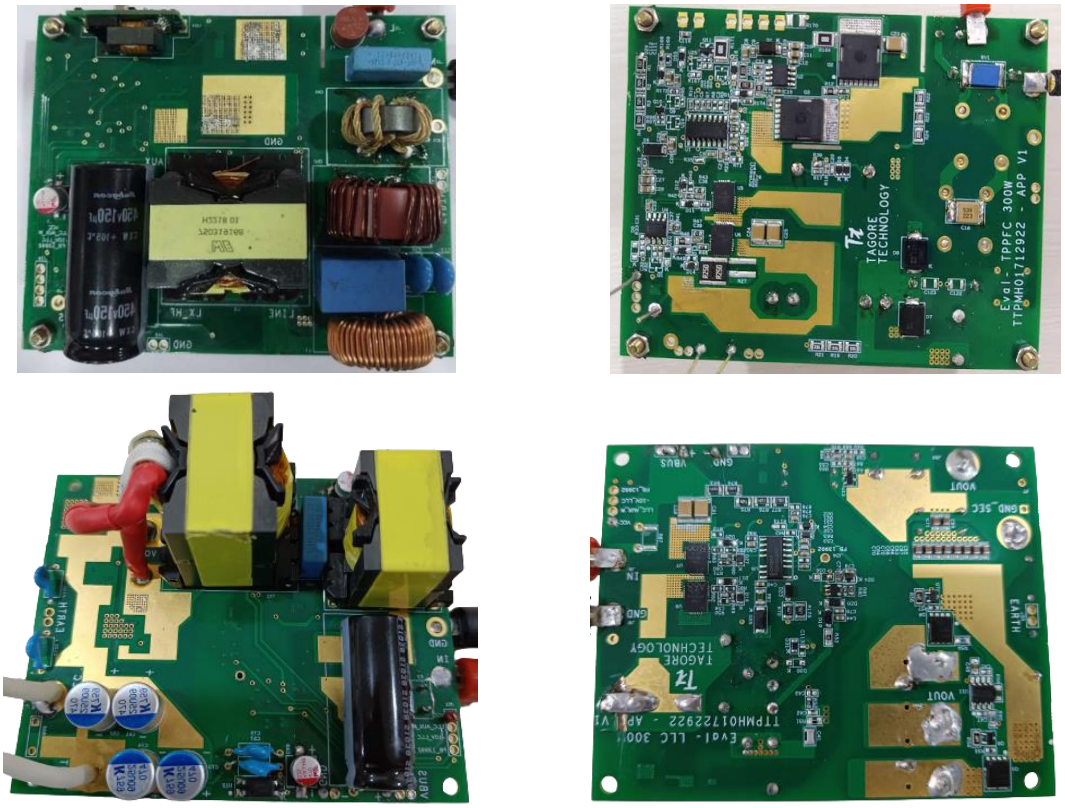

Figure 2: TPPFC power board (Top left and right) and LLC power board (Bottom left and right).

2.2 COMPONENT MARKUPS

The top and bottom side images of the TPPFC and LLC boards of the 300W EVB are shown in Fig. 2. For detailed component mark ups of the individual boards, please refer to the application notes TP44100SG-TPPFC240-EVB and TP44400SG-LLC240-EVB1 available at www.tagoretech.com.

2.3 TOPOLOGY AND FUNCTIONAL BLOCK DIAGRAM

The 300W EVB uses two-stage power conversion system as shown in Fig. 3. The first-stage uses a TPPFC topology, controlled by the onsemi's controller IC NCP1680. Tagore Technology's superior GaN FET TP44100SG has been used here. This stage is responsible for maintaining a 400 V regulated DC supply across its HV DC output terminals (DC link). It takes the necessary input power from the unregulated AC grid. It ensures near unity power factor, and low input current Total Harmonic Distortion (THD) at its AC input.

The second-stage uses an isolated half-bridge LLC resonant DC-DC converter topology, being controlled by the onsemi's controller IC NCP13992. Here the superior GaN FET TP44200SG serves as the main switching device. This stage takes the power from the DC link and processes it such a way that a regulated 20 V DC is maintained at the final output terminals throughout the load range.

The use of GaN FETs help significantly reduce the switching losses of both the converters, and increase the overall efficiency (η) of the power supply. For further details, please refer to the application notes *TP44100SG-TPPFC240-EVB* and *TP44400SG-LLC240-EVB1* at www.tagoretech.com.

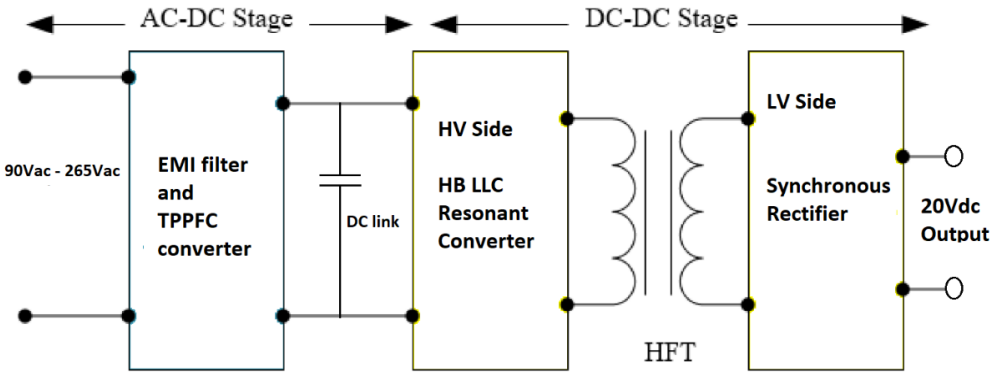

Figure 3: Block diagram representation of the 300W EVB.

2.4 SPECIFICATIONS

The key system specifications of the 300W EVB are given in Table 1.

Table 1: Key system specifications.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage	Output power = 240W	90	230	265	V_{RMS}
	Output power = 300W	110	230	265	V_{RMS}
Line frequency		47	50	63	*Hz*
OUTPUT CONDITIONS					
Output voltage			20		V_{DC}
Output current	$V_0 = 20V$			15	*A*
Output voltage ripple	$V_0 = 20V$ Peak -to- Peak	200	300	400	*mV*
Output power (nominal)				300	*W*
SYSTEM CHARACTERISTICS					
Peak efficiency	V_{DC} = 400V, Vac = 230V, V_0 = 20V, I_0 = 15A		96.2		*%*
Switching frequency (TPPFC)	V_{DC} = 400V, Vac = 230V, V_0 = 20V, I_0 = 15A		100	120	*kHz*
Switching frequency (LLC)			250	300	k Hz
Operating ambient temperature	Open frame	-10	25	55	^oC
Board dimensions (FR4 material, 4 layers)	Length × Width × Height	10.2 × 8.3 × 4.3 = 364			*cc*

3 CONNECTIONS AND START-UP PROCEDURE

This section describes a detailed connection diagram and start-up procedure for the 300W EVB.

3.1 OPERATING PROCEDURE

1. Take the 300W evaluation board TP44100SG-TPPFC+LLC300-EVB.
2. The list of equipment's needed for testing the evaluation board are as follows:
   a) Variac (for AC supply) – 1 no.
   b) Loading rheostat (or an electronic load if available) – 1 set
   c) Voltmeters/ammeters (DMM) – 2 nos.
   d) AC power analyzer – 1 no.

In order to test the 300W evaluation board, the following steps can be followed:

a) Ensure that the DC bus capacitors are discharged, and the output voltage is zero.
b) Make the electrical connections. Connect the DMMs at the AC input and DC output terminals. An example test setup is shown in Fig. 4.
c) Turn on the AC source (Variac) and gradually increase its output voltage from 0 Vac to 90 Vac at no load and beyond as per the specifications.
d) Observe that the output DC voltage is ~20 Vdc at the output of the EVB.
e) Adjust the loading rheostat or electronic load for different output power. Note the output power derating at low input voltage in the specification table.
f) Take all the measurements.
g) After conducting all the experiments, turn off the AC input power. Wait for some more time for the output DC bus to get discharged before touching the board.

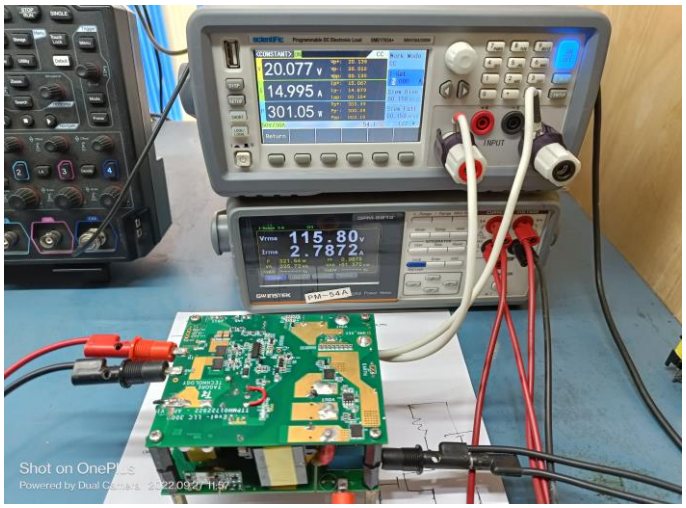

Figure 4: 300W Evaluation board test setup.

4 EXPERIMENTAL RESULTS

The 300W EVB has been tested with 90 V – 265 V AC input, and 0-15A load at 20 V output. The test results for the individual TPPFC and LLC modules are given in the application notes *TP44100SG-TPPFC240-EVB* and *TP44400SG-LLC240-EVB1* at www.tagoretech.com. This section presents some additional test results.

4.1 LOAD TRANSIENT WAVEFORMS

The 300W EVB has been tested for its load dynamic response. The effect of sudden application and removal of load on the output voltage is observed. The test results are shown in Fig. 5, where Vo is the output voltage and Io is the load current. No significant dip or overshoot is observed in the output voltage.

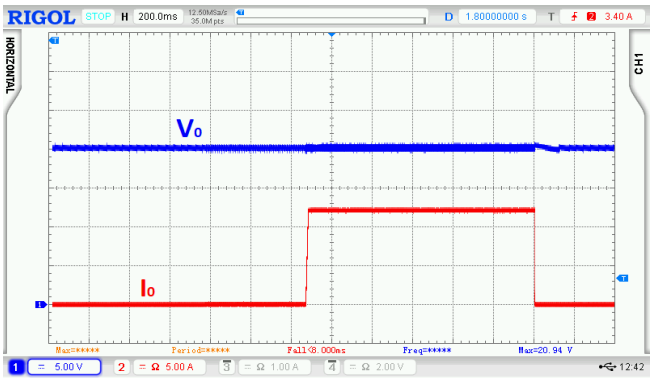

Figure 5: 300W EVB load dynamic response (0 to 100% load and vice-versa)

4.2 OUTPUT VOLTAGE RIPPLE (ΔVo)

The 300W EVB has been tested at no-load and full load. The voltage ripple on output voltage V_O (ΔV_O) is observed under both cases. These are depicted in below two subsections.

4.2.1 *V_o and ΔV_o at no-load*

Figure 6 represents the output voltage V_O and its ripple ΔV_O at no-load. The measured peak-to-peak ripple ΔV_O at no-load is less than 100 *mV*. The ripple can further be reduced by adding more electrolytic capacitors at the output.

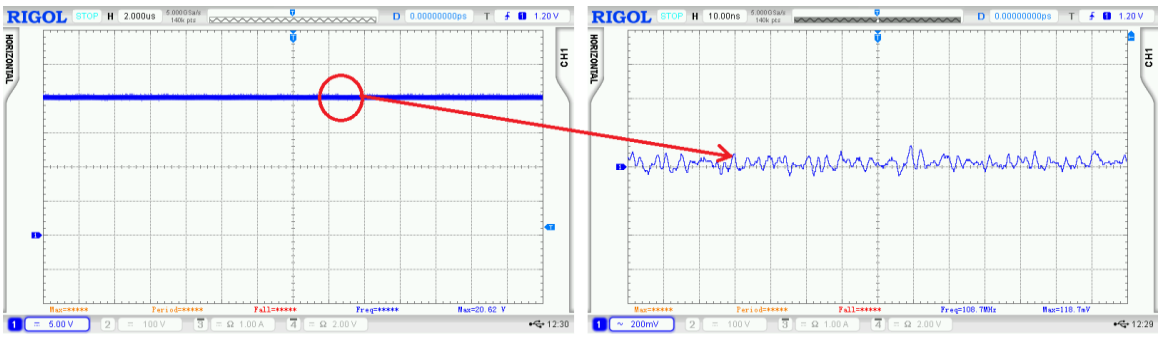

Figure 6: Output voltage Vo at no-load (left) and its corresponding ripple voltage ΔVo (right).

4.2.2 *Vo and ΔVo at full load*

The output voltage and its ripple corresponding to full load have been shown in Fig. 7. A peak-to-peak ripple ΔV_o of < 400 *mV* is observed, which can further be reduced by increasing the value of the output electrolytic capacitors as mentioned in the previous section.

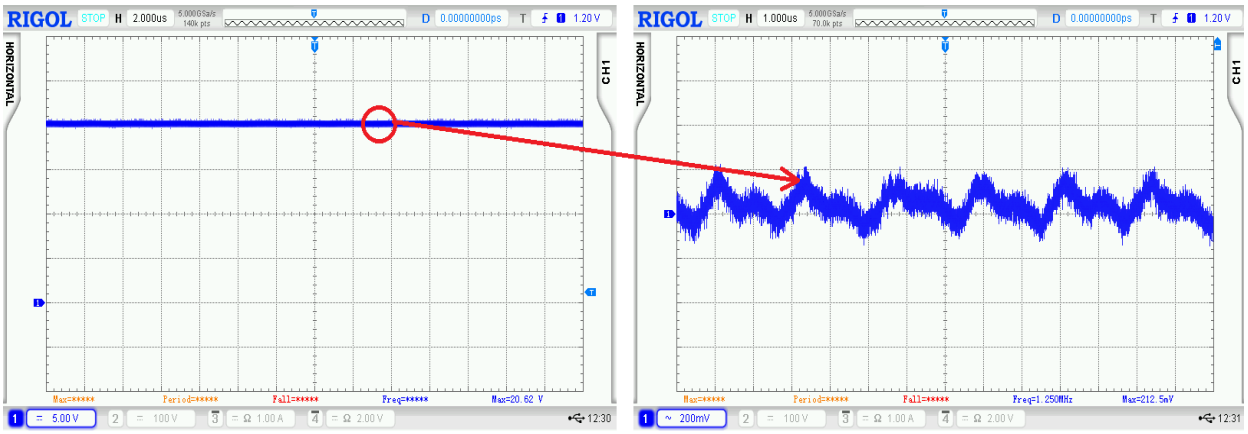

Figure 7: Output voltage Vo at full load (left) and its corresponding ripple voltage ΔVo (right).

5 PERFORMANCE DATA

5.1 EFFICIENCY DATA

The measured efficiencies versus output power at 115 Vac and 230 Vac inputs is shown in Fig. 8. The peak efficiency is 96.2%, which occurs at full load and at 230 V ac.

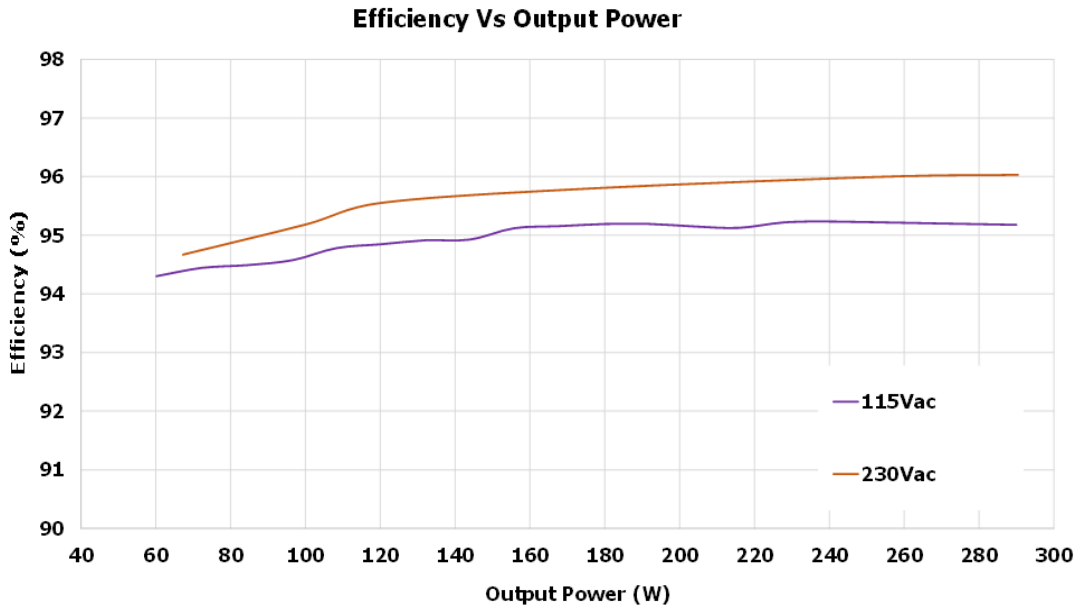

Figure 8: Efficiency vs output power at 115 Vac and 230 Vac inputs, and 20 V DC output.

5.2 LOAD REGULATION

The load current of the 300W EVB has been gradually increased from 0A to 15A, while recording the output voltage at the board terminal. The converter load regulation is shown in Fig. 9.

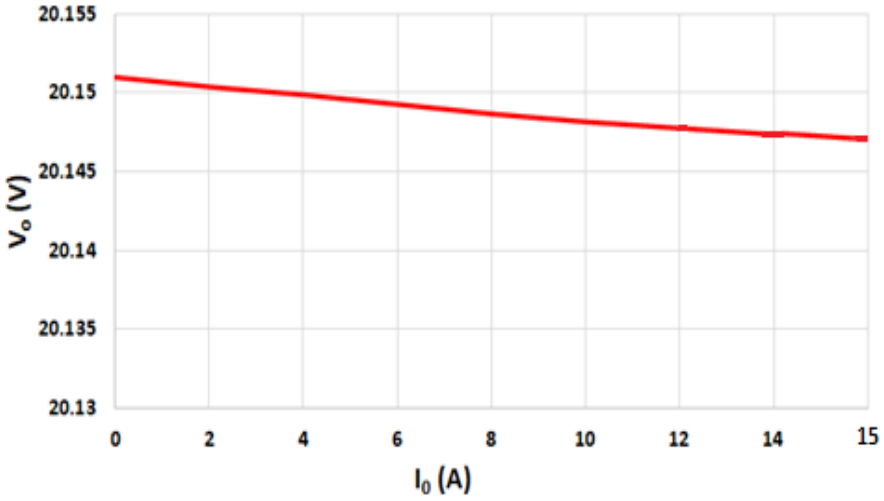

Figure 9: Output voltage vs load current.

5.3 THERMAL DATA

The thermal performances of the TPPFC and LLC boards up to 240W power have been presented in the application notes *TP44100SG-TPPFC240-EVB* and *TP44400SG-LLC240-EVB1* at www.tagoretech.com. Figure 10 shows the TPPFC and LLC GaN FET's case temperatures corresponding to test conditions of (a) 300W output power, (b) 20 Vdc output, (c) 115 Vac input (d) 25ºC ambient and (e) 45 mins of operation. The corresponding thermal images are shown in Fig. 11.

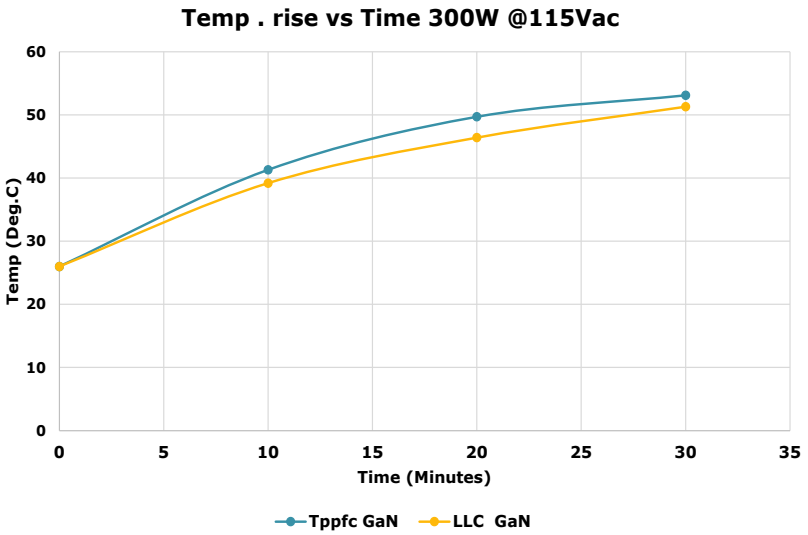

Figure 10: TPPFC and LLC GaN FET's case temperature rise over time under worst case scenarios.

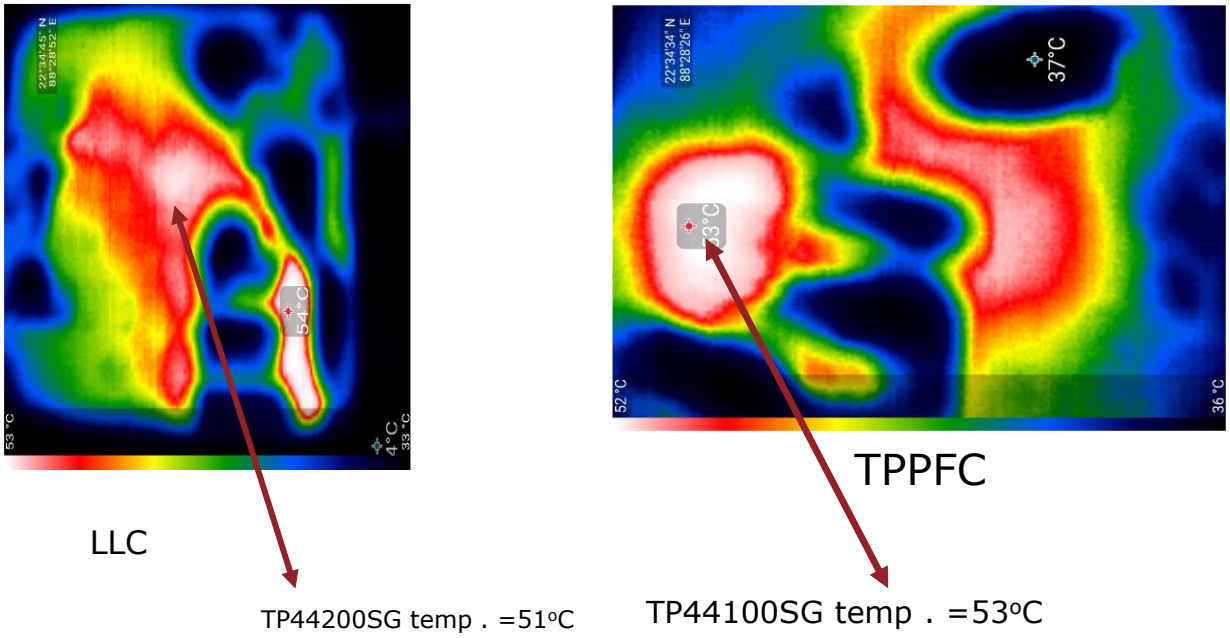

Figure 11: Thermal images of the bottom sides of TPPFC and LLC boards after 45 mins of operation.

6 PCB SCHEMATIC

Refer to the application notes TP44100SG-TPPFC240-EVB and TP44400SG-LLC240-EVB1 at www.tagoretech.com.

7 PCB LAYOUT AND ASSEMBLY

Refer to the application notes *TP44100SG-TPPFC240-EVB* and *TP44400SG-LLC240-EVB1* at www.tagoretech.com.

8 BILL OF MATERIALS

Refer to the application notes *TP44100SG-TPPFC240-EVB* and *TP44400SG-LLC240-EVB1* at www.tagoretech.com.

9 REVISION HISTORY

Document version	Date of release	Description of changes
Rev 1.0	16-Dec-22	First release